

# **AMT Emulator Board “Demoboard”**

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Demoboard is a simple circuit board, which essentially has LVDS receivers and transmitters and a core encoded into a XC4005E XILINX FPGA which provides the commands to be executed.

The main feature of the Demoboard is to emulate the output of the AMT TDC for testing communication with CSM-0. Essentially it sends serial streams of data to the CSM at LVDS levels after receiving a trigger from the CSM-0, just like a real TDC board would. The useful aspects are:

- ? According to the configuration loaded in it (the configuration can be chosen by selecting one of the four PROMs provided, as explained below). Since the data sent is hard coded into the configuration of the prom, one has perfect knowledge of data sent by the demoboard and hence knows what to expect to be seen by the CSM board.
- ? The fixed patterns from the demoboard permit us to focus on the CSM in cases where the data received is not as expected.
- ? Three identical patterns are sent from the demoboard permitting three channels of the CSM to be examined at once.

On the board we can easily recognize the Xilinx FPGA (in the center). The Xilinx XC17128E PROM is on its right. The board is powered by connecting a jumper (H2 on silkscreen) labeled with the VCC and GND sticker to a 5V source. The button in the upper portion of the board is the reset button. By pushing it, all the commands and data outputs are reset and the board is set in the state to begin anew. It is recommended that the board be reset every time any cable is plugged or unplugged. The is sensible to very short (in time) pulses and can easily misunderstand cable removal and/or reconnection and start to sending serial data.

The picture below shows the demoboard with 2 cables inserted.



In the left part of the board there are three shielded RJ45 plugs for the connection to the CSM through RJ45 cables. According to the number of these connections to the CSM-0, the demoboard can emulate one, two or three TDC's. The data sent out from the three connections are absolutely the same so the CSM-0 will appear to be connected to TDC boards sending identical data. The clock of the whole board is taken from one of the 40MHz clock lines received from the CSM-0. **WARNING:** As the clock is taken only from the first connection (the one in the board upper left corner), it is always **NECESSARY** to use this particular plug when working with the demoboard.

The FPGA instruction setting (*bitfile*) is stored and downloaded from a PROM, plugged in a dip 8 socket. By changing the PROM

(manually unplug/plug) different output streams can be sent. Four PROMs are provided with each Demoboard, each labeled with a number (1 through 4). The following list explains the output specific to each of the numbered PROMS.

1. *Democont1* sends 99 data words serially in LVDS mode, beginning with the code 0011. This occurs every time it receives a trigger from CSM-0 board (after the first trigger following a reset phase 100 words are sent).
2. *Democont2* sends continuously data words serially in LVDS mode, beginning with the code 0011 as soon as it receives the first trigger from CSM0 board. The effective frequency of these words is 100 KHz obtained by adding a pause period between each 2 consequent data streams.
3. *Demosimple* sends 6 data words serially in LVDS mode every time a trigger is received from CSM-0 board. The data word order is the following:
  - ? *TDC header* (MSB = 1010);
  - ? Data word whose MSB are 0010;
  - ? Data word whose MSB are 0011;
  - ? Data word whose MSB are 0100;
  - ? Data word whose MSB are 1111;
  - ? *TDC trailer* (MSB = 1100).

Note: The CSM-0 does not accept data words beginning with code “F” (the 5<sup>th</sup> one), and will discard it.

4. *Demochan* sends 98 data words serially in LVDS mode every time a trigger is received from CSM0 board. The data word order is the following:
  - ? *TDC header* (MSB = 1010);
  - ? 2 data words beginning with the code 0011 for each of the 24 channels;
  - ? 2 data words beginning with the code 0100 for each of the 24 channels;
  - ? *TDC trailer* (MSB = 1100).

The total number of words sent out is therefore 98 for each trigger.

For further information about the functions specific to the PROM used, VerilogHDL code files created and synthesized for the FPGA download are provided with this document. They have been called *demoboard\_1* through *4* according to the version they implement.

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